1-13. (Cancelled)

14. (Currently Amended) A stacked package for electronic elements, comprising:

a substrate, having a supporting surface, wherein a plurality of stud bumps are formed on the supporting surface by a stud bump process and contact the supporting surface; and

a plurality of electronic elements, each having a plurality of vias corresponding to the stud bumps, wherein the vias of each electronic element are respectively aligned with the stud bumps, each of the stud bumps being allowed to pass through the corresponding vias of the plurality of electronic elements so as to securely mount and stack the electronic elements on the substrate; and

a solder paste that is applied over exposed surfaces of the stud bumps on the topmost electronic element, the solder paste being reflowed to flow down through the vias along the stud bumps so as to securely connect the electronic elements.

CLAIMS 15-16 (CANCELLED)

17. (Original) The stacked package for electronic elements of claim 14, further comprising a spacer between adjacent electronic elements.

18. (Original) The stacked package for electronic elements of claim 14, wherein the material of the stud bumps is a conductive metal.

19. (Original) The stacked package for electronic elements of claim 14, wherein the material of the stud bumps is gold, copper or aluminum.

20. (Original) The stacked package for electronic elements of claim 14, wherein the element is a silicon chip, a GaAs chip, an InP chip or a epitaxily-grown chip.

21. (Original) The stacked package for electronic elements of claim 14, wherein the substrate is an organic substrate, a ceramic substrate, a glass substrate, a silicon substrate or a GaAs substrate.

22. (Cancelled)

23. (Cancelled)

24. (Previously Presented) The stacked package for electronic elements of claim 14, wherein each of the stud bumps has a bottom wider than a width of the corresponding vias of the plurality of electronic elements.

25. (Previously Presented) The stacked package for electronic elements of claim 14, wherein the plurality of electronic elements are stacked from bottom to top as a stacked structure, and each of the stud bumps has a height larger than a height of the stacked structure.

26. (Previously Presented) The stacked package for electronic elements of claim 14, wherein the plurality of electronic elements are stacked from bottom to top as a stacked structure, and each of the stud bumps protrudes from a top surface of the topmost electronic element of the stacked structure.

27. (Cancelled)

28. (Previously Presented) A stacked package for electronic elements, comprising:

a substrate, having a supporting surface, wherein a plurality of stud bumps are formed on the supporting surface by a stud bump process;

a plurality of electronic elements, each having a plurality of vias corresponding to the stud bumps, wherein the vias of each electronic element are respectively aligned with the stud bumps, the stud bumps being allowed to pass through the vias so as to securely mount and stack the electronic elements on the substrate; and

a conductive glue that is applied over the stud bumps on an exposed surface of the topmost electronic element, and flows through the vias along the stud bumps so as to securely connect the electronic elements.

29. (New) The stacked package for electronic elements of claim 28, further comprising a spacer between adjacent electronic elements.

30. (New) The stacked package for electronic elements of claim 28, wherein the material of the stud bumps is a conductive metal.

31. (New) The stacked package for electronic elements of claim 28, wherein the material of the stud bumps is gold, copper or aluminum.

32. (New) The stacked package for electronic elements of claim 28, wherein the element is a silicon chip, a GaAs chip, an InP chip or a epitaxily-grown chip.

33. (New) The stacked package for electronic elements of claim 28, wherein the substrate is an organic substrate, a ceramic substrate, a glass substrate, a silicon substrate or a GaAs substrate.

34. (New) The stacked package for electronic elements of claim 28, wherein each of the stud bumps has a bottom wider than a width of the corresponding vias of the plurality of electronic elements.

35. (New) The stacked package for electronic elements of claim 28, wherein the plurality of electronic elements are stacked from bottom to top as a stacked structure, and each of the stud bumps has a height larger than a height of the stacked structure.

36. (New) The stacked package for electronic elements of claim 28, wherein the plurality of electronic elements are stacked from bottom to top as a stacked structure, and each of the stud bumps protrudes from a top surface of the topmost electronic element of the stacked structure.